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MOSFET Scaling and Small Geometry Effects

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Abstract

There have been proposed several sets of “rules” for scaling, for the purpose of discovering as much as possible the electrical consequences of MOSFET size reduction. Principle am There have been proposed several sets of “rules” for scaling, for the purpose of discovering as much as possible the electrical ong these are rules by Dennard in 1974 (1 µm channel length) and Baccarani in 1984 (0.25 µm).

By scaling, we hope to… -Increase packing density and chip functionality, Increase device current and speed. Lower cost (increase cost effectiveness). but the trade-offs are Mobility degradation due to increased vertical fields. Velocity saturation due to increased lateral fields, Charge sharing by drain (short channel effects; DIBL), Increased drain/source resistance due to reduced area for current flow.

Keywords: Silicon-on-Insulator (SOI), MOSFETs, Short-channel effects, modeling,Simulation

Introduction

IN ORDER TO realize higher speed and higher packing density MOS integrated circuits, the dimensions of MOSFETs have continued to shrink according to the scaling law proposed by Dennard et al. [1]. Yet, the power consumption of modern VLSIs has become rather significant as a result of extremely large integration. Reducing this power is strongly desired. Choosing a lower power supply voltage is an effective method. However, it leads to the degradation of MOSFET current driving capability. Consequently, scaling of MOS dimensions is important in order to improve the drivability, and to achieve higher performance and higher functional VLSIs.

With aggressive technology scaling to enhance performance, circumventing the detrimental short-channel effects (SCE) to improve the device reliability has been the focus in MOSFET scaling. When the channel length shrinks, the controllability of the gate over the channel depletion region reduces due to the increased charge sharing from source/drain. SCE leads to several reliability issues including the dependence of device characteristics, such as threshold voltage, upon channel length. This leads to the scatter of device characteristics because of the scatter of gate length produced during the fabrication process. The predominating reliability problems associated with SCE are a lack of pinchoff and a shift in threshold voltage with decreasing channel length as well as drain-induced barrier lowering (DIBL) and hot-carrier effect at increasing drain voltage. Moreover, SCE degrades the controllability of the gate voltage to drain current, which leads to the degradation of the subthreshold slope and the increase in drain off-current. This degradation is described as charge sharing by the gate and drain electric fields in the channel depletion layer in Poon and Yau’s model [2], which was reported as the first SCE model. Thinning gate oxide and using shallow source/drain junctions are known to be effective ways of preventing SCE. With short-channel devices, the reliability margins have also been cut down significantly [3]. Particularly, the high electric field near the drain becomes more crucial and poses a limit on device operation, notably by a large gate current, substrate current and a substantial threshold voltage shift [4]–[5]. Efforts have been made to model the device degradation due to hot electron generation [6]–[7].

This description can be applied to conventional MOSFETs fabricated in a bulk silicon wafer. What about thin-film SOI MOSFETs? They are attractive devices for low-power high-speed VLSI applications because of their small parasitic capacitance [8]. Young [9] analyzed the SCE using a device simulator, and concluded that SCE is well suppressed in thin-film SOI MOSFETs when compared to bulk MOSFETs. In general, it is believed that thin-film SOI MOSFETs have a higher immunity

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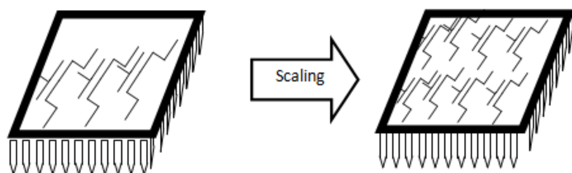
to SCE compared with bulk MOSFETs. This may be due to the difference in source/drain junction depths between the two kinds of devices. For instance, the thickness of the silicon film, tSi , which corresponds to the source/drain junction depth of 50–100 nm, is common in 0.25–0.35-µm SOI MOSFETs. It is extremely shallow compared with the junction depth of 100–200 nm in 0.25–0.35- µm gate bulk MOSFETs. However, to take advantage of the ameliorated SCEs in deep-submicron fully depleted SOI, tSi must be considerably smaller than the source/drain junction depth (tSi ~ 10-15nm). Moreover, a strong coupling through the buried oxide in thin-film devices exists, and consequently, very thin buried oxides (tb ~100 nm) are needed which trades off with junction capacitance considerations. With the gate length scaling approaching sub-100-nm regime for improved performance and density, the requirements for body-doping concentration, gate-oxide thickness, and source/drain (S/D) doping profiles to control SCEs become increasingly difficult to meet when conventional device structures based on bulk silicon substrates are employed. Moreover, SOI brings in new reliability issues, which are not known in the traditional bulk-Si devices, related to the presence of the buried oxide like self-heating and hot-electron degradation of the buried oxide. In a high electrical field of a short channel transistor, carriers may gain enough energy and get trapped in the buried oxide along with the gate oxide. The buried oxide is more subject to degradation than the gate oxide because the high density of electron traps is an intrinsic feature of SIMOX oxides. These defects may change parameters of the back channel in the field-effect transistor (FET) and affect the performance of CMOS circuit through the coupling effect. Thus, the hot-carrier-induced degradation in SOI devices is more complex than that in bulk devices because of the thin-film effects and the existence of two interfaces (two oxides and two channels). Hence, for small-geometry SOI CMOS devices, SCEs are becoming increasingly important [10]–[11].

MOSFET Channel Scaling Discusion

To increase the number of devices per IC, the device dimensions had to be shrunk from one generation to another (i.e. scaled down)



- In theory, there are two methods of scaling:

Full-Scaling (also called Constant-Field scaling): In this method the device dimensions (both horizontal and vertical) are scaled down by 1/S, where S is the scaling factor. In order to keep the electric field constant within the device, the voltages have to be scaled also by 1/S such that the ratio between voltage and distance (which represents the electric field) remain constant. The threshold voltage is also scaled down by the same factor as the voltage to preserve the functionality of the circuits and the noise margins relative to one another. As a result of this type of scaling the currents will be reduced and hence the total power per transistor (P=IxV) will also be reduced; however the power density will remain constant since the number of transistors per unit area will increase. This means that the total chip power will remain constant if the chip size remains the same (this usually the case).

The table below summarizes how each device parameter scales with S (S>1)

Parameter	Before scaling	After scaling
Channel length	L	L/S
Channel width	W	W/S
Oxide thickness	tox	tox/S
S/D junction depth	Xj	Xj/S
Power Supply	VDD	VDD/S
Threshold voltage	VTO	VTO /S
Doping Density	NA & ND	NA *S and ND *S
Oxide Capacitance	Cox	S*Cox
Drain Current	IDS	IDS /S
Power/Transistor	P	P/S2
Power Density/cm2	p	p

Constant-Voltage scaling (CVS): In this method the device dimensions (both horizontal and vertical are scaled by S, however, the operating voltages remain constant. This means that the electric fields within the device will increase (filed =Voltage/distance). The threshold voltages remain constant while the power per transistor will increase by S. The power density per unit area will increase by S3! This means that for the same chip area, the power chip power will increase by S3. This makes constant-voltage-scaling (CVS) very impractical. Also, the device doping has to be increased more aggressively (by S2) than the constant-field scaling to prevent channel punch-through. Channel punch-through occurs when the Source and Drain Depletion regions touches one another. By increasing the doping by S2, the depletion region thickness is reduced by S (the same ratio as the channel length). However, there is a limit for how much the doping can be increased (the solid solubility limit of the dopant in Silicon). Again, this makes the CVS impractical in most cases.

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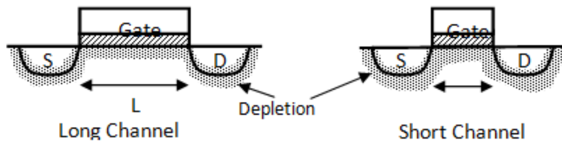
The following table summarizes the changes in key device parameters under constant-voltage scaling:

Parameter	Before scaling	After scaling
Channel length	L	L/S
Channel width	W	W/S
Oxide thickness	tox	tox/S
S/D junction depth	Xj	Xj/S
Power Supply	VDD	VDD
Threshold voltage	VTO	VTO
Doping Density	NA & ND	NA * S2 and ND * S2
Oxide Capacitance	Cox	S*Cox
Drain Current	IDS	IDS * S
Power/Transistor	P	P*S
Power Desity/cm2	p	p * S3

Small Geometry Effects

Short channel effects start to appear as the channel length becomes less than 10 times the depletion region width of the source/drain regions. The figure below demonstrates the difference between long and short channel transistors.



- The major short-channel effects are:

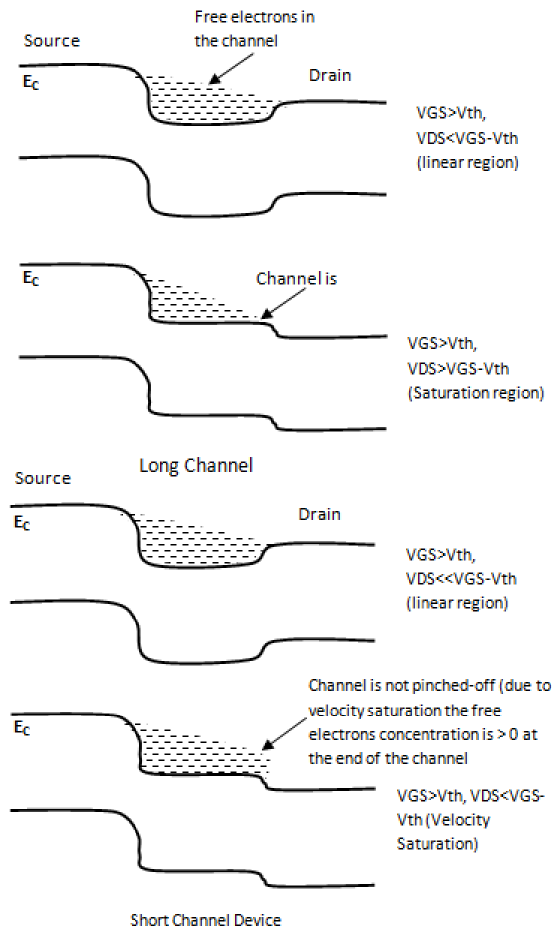
Carrier Velocity Saturation

Recall that the mobility determines the increase in carrier velocity as the electric field increases. But this does not continue forever. As the channel length is reduced, the horizontal electric field between the source and drain increases to a point where the carrier mobility becomes zero, i.e. the carrier velocity won't increase beyond a certain limit (hence the term velocity saturation). Once velocity saturation sets in, the drain current won't increase as V_{DS} increases even if V_{DS} is still < $V_{GS} - V_{th}$. The figure below shows the effect of velocity saturation using energy band diagram of an NMOS transistor.

In the limit the short-channel device will have a saturation current of:

$$I_{DSat} = Cox*W*Vsat* V_{DSat}$$

Where Vsat is the saturation velocity (~2E7 cm/s) and VDSat is the drain to source voltage at the on-set of velocity saturation and depends on L and the substrate doping (semi-



empirical formulae are used to determine this voltage). However, for most devices they will have a saturation current characteristic between those of long and short channel devices:

$$I_{DSat} = Cox*W*K\ (V_{GS} - V_{th})^n$$

Where K and n are constants that are obtained from semi-empirical formulae, 1<n<2 (typically, n is between 1.3 to 1.4). This means that the saturation current won't increase with VGS in a quadratic relation, but rather close to a linear relation, which reduces the speed. Also, once the channel length L goes below the velocity saturation limit, the drain current won't increase with reducing L further, a major set back for scaling efforts (i.e. circuits won't get faster as before with scaling).

Threshold Voltage Reduction

Since for the short-channel devices, a relatively large portion of the channel depletion charge QB is controlled by the drain, a smaller amount of gate voltage is required to achieve strong inversion and create the channel, i.e. the threshold voltage will be smaller. The following figure illustrates this.

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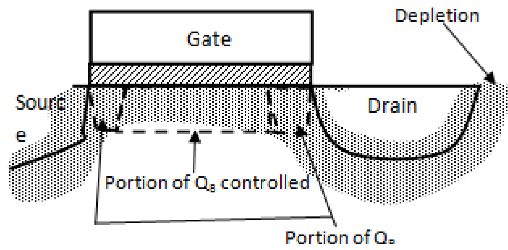
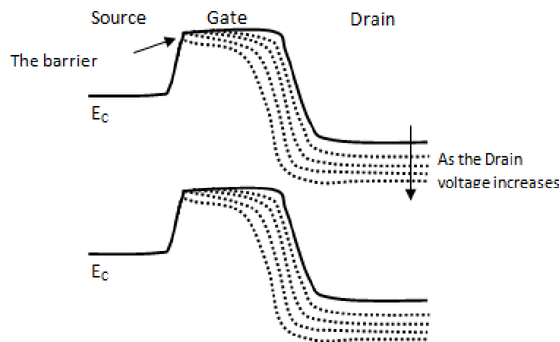


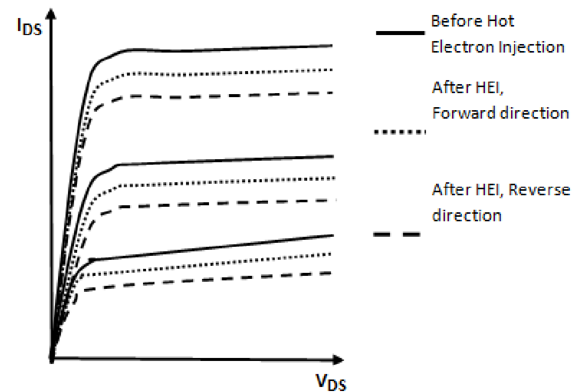
Drain-Induced-Barrier-Lowering (DIBL)

Because of the short channel length, the drain voltage will reduce the potential barrier between the source and substrate. Hence it become easier for carriers at the source to jump over this barrier and drift to the drain even at the absence of a channel (i.e. when the gate to source voltage is less than the threshold voltage). The DIBL effect causes the MOS devices to "leak" currents when they are turned-off. These currents are called leakage currents or off-currents. If the DIBL effect increases significantly, the MOS switch may become always ON, i.e. it is not controlled by the gate any more. This condition would occur if the source and drain depletion regions reach one another, a condition called punch-through. Increasing the substrate doping under the gate/channel reduces the DIBL effect. The figure below demonstrates the DIBL effect using energy band diagram.



Hot Electron Injection into the Gate Oxide

Due to the high electric fields that result in short-channel devices, electrons can attain enough speed to jump over the energy barrier between the Si channel region and the gate oxide. Once they are injected into the oxide, they become part of its trapped charge. As it is already known, this would alter the device's threshold voltage and may render the device totally useless with time. Also, since the injection occurs near the drain side, where the electrons would have attained the highest speed, the device operation becomes asymmetrical, i.e. the I-V characteristics will exhibit direction dependency. This is because the threshold if the current is flowing from the source to the drain (forward direction) is smaller than the threshold in the reverse direction. The figure below shows the effects of HE injection on the I-V characteristics of an NMOS device.



Effects of Hot Electron Injection (HEI) on NMOS I-V characteristics

Conclusion

With the continuous scaling of CMOS devices, leakage current is becoming a major contributor to the total power consumption. In current deep-submicrometer devices with low threshold voltages, subthreshold and gate leakage have become dominant sources of leakage and are expected to increase with the technology scaling. GIDL and BTBT may also become a concern in advanced CMOS devices. To manage the increasing leakage in deep-submicrometer CMOS circuits, solutions for leakage reduction have to be sought both at the process technology and circuit levels. At the process technology level, well-engineering techniques by retrograde and halo doping are used to reduce leakage and improve short-channel characteristics. At the circuit level, transistor stacking, multiple , dynamic, multiple, and dynamic techniques can effectively reduce the leakage current in high-performance logic and memory designs.

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